[0060] **FIG. 8** shows another embodiment of a HEMT **100** according to the present invention that is similar to the HEMT **10** shown in **FIGS. 1 and 2** and has a substrate **12**, nucleation layer **14**, buffer layer **16**, barrier layer **18**, source electrode **20**, drain electrode **22**, gate **24**, 2DEG **26** and first spacer layer **28**. However, instead of having a single first field plate, it has a first field plate that is separated into a source field plate **102** and a drain field plate **104**. The source field plate **102** overlaps the source side of the gate **24** and extends a distance L_{fs} on the spacer layer **28** toward the source electrode **20**, with L_{fs} being in the range of distances described above. The drain field plate **104** overlaps the gate **24** and extends a distance L_{fd} on the spacer layer **28** toward the drain contact **22**, with L_{fd} being in the range of distances described above. The source and drain field plates **102**, **104** can each be connected to the source contact **20** or the gate **24** (using the methods described above), or one can be connected to the source contact **20** and the other connected to the gate **24**.

[0061] In different embodiments, the source and drain field plates **102**, **104** do not need to overlap the gate **24**, and one or both can have a gap between the edge of the gate and the edge of the field plate. Overlapping of the gate can introduce additional capacitance that can negatively impact performance. For source and drain field plates to effectively reduce the electric field, a gap between the edge of the gate and the field plates must be relatively small, which can present some difficulties during fabrication. By having the field plates **102**, **104** overlap the gate **24**, the HEMT can be fabricated without having to meet the tolerances of this small gap. In determining whether to use an overlapping field plate or non-overlapping field plate, the ease of manufacturing is balanced with the reduced capacitance.

[0062] The structures of the present invention can also be used in other types of transistors made of different material systems. **FIG. 9** shows one embodiment of a MESFET **110** according to the present invention that is silicon carbide based. MESFET **110** comprises a silicon carbide substrate **112** on which a silicon carbide buffer **114** and a silicon carbide channel layer **116** are formed with the buffer **114** sandwiched between the channel layer **116** and substrate **112**. The buffer **114** and channel layer **116** generally form the MESFET's active region. Source and drain electrodes **118**, **120** are formed in contact with the channel layer **116** and a gate **122** is formed on the channel layer **116** between the source and drain electrodes **118**, **120**. In the preferred embodiment, the gate **122** is recessed in the channel layer **116**, although it can also be on the channel layer **116** without recess as long as adequate electrical contact is made between the two. The gate **122** can also be partially recessed, with only part of its bottom surface recessed in the channel layer **116**.

[0063] A non-conducting (dielectric) spacer layer **124** is formed over the gate **122** and the surface of the channel layer **116** between the gate **122** and the source and drain electrodes **118**, **120**. Similar to the spacer layer **28** described above and shown in **FIGS. 1 and 2**, the spacer layer **124** can comprise a layer of non-conducting material such as a dielectric, or a number of different layers of non-conducting materials such as different dielectrics.

[0064] A first field plate **126** is formed on the spacer layer **124** between and over the gate **122** and extends a distance L_{fs} on the spacer layer **124** toward the source electrode **118**, and a distance L_{fd} toward the drain electrode **120**, both in the range of distances described above. The field plate **126** can also be connected to either the source electrode **118** or the gate **122** using the same connecting structures as described above. The first field plate can also comprise more than one field plate, such as the two piece drain field plate and source field plate arrangement described above.

[0065] A second non-conducting spacer layer **128** (in phantom) can be formed over the first field plate **126** and first spacer layer **124** and is similar to second spacer layer **40** described above and shown in **FIG. 3**. Similarly, a second field plate **130** (in phantom) is provided on the second spacer layer **128**, and is similar to the second field plate **42** described above and shown in **FIG. 3**, and is similarly connected.

[0066] **FIG. 10** shows another embodiment of a silicon carbide MESFET **140** according to the present invention that has similar features of the MESFET **110** in **FIG. 9**, including a substrate **112**, buffer **114**, channel layer **116**, source electrode **118**, drain electrode **120**. A recessed gate **142** is formed on the channel layer **116** between the source and drain electrodes **118**, **120**, although it can also be on the channel layer **116**. MESFET **140** also comprises a spacer layer **144** that does not overlap the gate **142**, but covers at least part of the surface of the channel layer **116** between the gate **142** and the source and drain electrodes **118**, **120**. Field plate **146** is formed integral with the gate **142** and extends a distance L_{fs} on the spacer layer **144** toward the source electrode **118**, and a distance L_{fd} toward the drain electrode **120**, both in the range of distances described above. The spacer layer **144** can be a dielectric material and in those instances where the spacer layer **144** is formed before device metallization, the spacer layer can comprise an epitaxial material as described above.

[0067] **FIG. 11** shows a table **130** comparing the operating characteristics of GaN based HEMT (Device A) with no gate-source field plate compared to the operating characteristics of a GaN based HEMT (Device B) with a gate-source field plate having a length of 0.2 microns. The measurements of Device A and B were taken in reference to power degradation at 200C class-C operation for 10 hours with Vg=−7V at 4 gigahertz (GHz) driven to 1 decibel (dB) compression. The measurements show breakdown in Device A, while Device B does not experience breakdown under the same conditions.

[0068] It is understood that the field plate arrangement can be applied to other transistors beyond HEMTs and MESFETs, with one example being a Metal Oxide Semiconductor Heterostructure Field Effect Transistor (MOSHFET). In MOSHFETS, the spacer layer can be formed between the gate and the MOSHFETs active region. The spacer layer can be partially removed from under the gate so that the gate is on a then spacer (insulator) layer while the field plate is on a thicker spacer (insulator) layer. The gate would still be "in contact" with the active region through the insulator layer, with the MOSHFET arrangement designed to reduce gate leakage.

[0069] The embodiments above provide wide bandgap transistors with improved power at microwave and millimeter wave frequencies. The transistors exhibit simultaneous high gain, high power, and more stable operation due to